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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WERNER, DAVID N	

ART UNIT	PAPER NUMBER
2483	

MAIL DATE	DELIVERY MODE
11/23/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/765,813	RAMAKRISHNAN, LAKSHMANAN	
	Examiner	Art Unit	
	DAVID N. WERNER	2483	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-12,20,21 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-12,20,21 and 23* is/are rejected.

7)☒ Claim(s) *23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 December 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The Art Unit location of your application in the U.S.P.T.O. has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Art Unit 2483.

2. This Office action for U.S. Patent Application No. 10/765,813 is responsive to the Request for Continued Examination filed 12 October 2010, in reply to the Final Rejection of 12 July 2010. Claims 9–12, 20, 21, and 23 are pending. Of those, Claim 23 is new.

3. In the previous Office action, Claims 9–12 and 20–21 were rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent Application Publication No. 2002/0080870 A1 ("Piazza") in view of U.S. Patent Application Publication No. 2002/0174305 A1 ("Vartti").

Response to Arguments

4. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection. Without conceding that Applicant's argument that the specific use of a "macroblock row" capacity of a local buffer was not obvious in view of other buffers having other sizes in general was correct, U.S. Patent No. 5,414,468 A ("Lee"), cited but not relied on in the previous Office action, is introduced to the claim rejections as an example of a "macroblock row" buffer used in the art at the time of the present invention.

Claim Objections

5. Claim 23 is objected to because of the following informalities: the word "and" should be added to the end of the second from final indentation, and in the final line, the word "engine" is misspelled as "engin". Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 9–12, 20, 21, and 23 rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2002/0080870 A1 ("Piazza") in view of U.S. Patent Application Publication No. 2002/0174305 A1 ("Vartti") and in view of U.S. Patent No. 5,414,468 A ("Lee").

Piazza teaches a video decoder with motion compensation. Regarding Claim 9, Figure 8 of Piazza illustrates a block diagram of the decoder. Included is memory 830 storing compressed macroblock 880. Piazza, ¶ 0065. The compressed macroblock is then loaded into cache memory 810. Id. at ¶ 0066. Cache memory 810 is the claimed "local buffer". Processor 800 then processes the data in cache memory 810 and performs decoding operations such as inverse DCT. Id. at ¶ 0067. Then, Processor 800 is the claimed "decompression engine". However, the present invention differs from Piazza in two factors. First, the present invention discloses an extractor for direct

memory access engine control of the local buffer, giving instructions that the compressed data stored in the buffer may be overwritten by more compressed video data, not disclosed in Piazza. Second, the present invention is directed to a processor having a local buffer that stores "a macroblock row" whereas cache memory 810 in Piazza only appears to store a single macroblock.

First, regarding the claimed extractor, it is respectfully submitted that Vartti discloses this limitation, and it would have been obvious to one having ordinary skill in the art at the time of the present invention to modify the Piazza decoder to include the claimed extractor taught by Vartti.

Vartti teaches a system for controlling cache memory. Regarding Claim 9, figure 3 illustrates a flowchart of the memory locking process. At step 300, a processor requests a "storage lock" on a cache line. Vartti, ¶ 0049. The lock grants the processor the exclusive access to the cache line so that no other processor or memory unit may access it. Id. at ¶ 0005. This exclusivity includes a right to exclude other processors or memory units from overwriting the line. Id. at ¶¶ 0045, 0037. The ownership may additionally be a read-only type, in which the owner may read the line, but no other requester may access the line at all. Id. at ¶ 0043. As applied to the present invention, when the decompression engine locks the buffer that stores the "portion", the buffer cannot be overwritten by another component of the decoder.

At step 302 of Vartti, the system determines if the requested cache line is owned by another requester or if it is clear for the current requester. Vartti at ¶ 0049. If the cache line is clear or if the current requester already owns the line, the request from step 300 is granted at step 306. Id. at ¶ 0050. The processor is then free to use the

data in the cache subject to the conditions of the ownership, such as read-only. Id. at ¶ 0051. As applied to the present invention, the processing required during ownership is decompressing the data portion stored in the buffer. After the processor is finished using the data, it issues a "release lock notification" at step 308. Id. This release lock notification is the claimed "indicator" allowing further processing of the cache data, such as overwriting. Figure 1 illustrates the computing system of Vartti as a whole as a massively parallel or distributed environment, and figure 2 illustrates an example of one processing module. Id. at ¶ 0024. Included in the processing module is an instruction processor 202 that performs the actual processing operations, cache 206, and storage controller 204 that interfaces between the processor and the cache. Id. at ¶ 0025. Then, the cache 206 is the claimed "local buffer", processor 202 is the claimed "decompression engine", and controller 204 is the claimed "extractor".

Piazza discloses a majority of the claimed invention except for determining when it is "safe" to overwrite a buffer memory. Vartti teaches that it was known to "lock" a cache memory to allow one processor to read its contents as needed and no other component of a system to access it during the time the memory is locked. Therefore, it would have been obvious to one having ordinary skill in the art at the time of the present invention to modify the cache memory of Piazza to be lockable when the processor is decoding the data stored within, as in the cache memory of Vartti, since Vartti states in paragraph 0004 that such a modification would prevent processing errors from inconsistent or incoherent data that changes during processing.

Second, regarding the size of the buffer as storing "a macroblock row", it is respectfully submitted that Lee discloses this limitation, and it would have been obvious

to one having ordinary skill in the art to modify the Piazza decoder further to include a macroblock-row-sized buffer.

Lee teaches a video decoder. Regarding Claim 9, in Lee, fig. 1 illustrates the decoder, including buffer system 400. Included in buffer 400 is frame buffer 410, slice buffer 420, and macroblock buffer 430. Since the technical term in the art for a "macroblock row" or "row of macroblocks" is a slice, the "slice buffer" 420 of Lee is considered to store a macroblock row, as claimed. The Lee decoder performs variable-length decoding of video data one slice at a time, storing the partially-decoded slices in a buffer before fully decoding their coefficient data. Lee, col. 4: lines 36–44. This is the claimed process of decoding compressed video data stored in the macroblock row local buffer.

Piazza, in combination with Vartti, discloses the claimed invention except for a macroblock-row sized local buffer. Lee teaches that it was known in the art at the time of the present invention to use a macroblock row, or slice, buffer to store partially-decoded video data for full decoding. Therefore, it would have been obvious to one having ordinary skill in the art at the time of the present invention to modify the system of Piazza to use a macroblock-row sized buffer, as taught by Lee, since Lee states in col. 1: line 38–col. 2: line 18 that such a modification would eliminate a processing bottleneck at entropy decoding macroblock row units of data.

Regarding Claim 10, in Piazza, a macroblock command to data stored in cache memory 810 is the claimed command. Piazza, ¶ 0087.

Regarding Claim 11, in Lee, assuming only one slice is in slice buffer 420 at once, a second slice after the first slice is processed and stored in the slice buffer 420 is the claimed "another portion of the compressed video data".

Regarding Claim 12, as previously mentioned, figure 1 of Vartti illustrates a parallel embodiment with multiple caches and processors.

Regarding Independent Claim 20, as discussed above, in Piazza, processor 800 is the claimed video decoder and cache 810, as scaled up to hold a slice or macroblock row, is the claimed local buffer. In Vartti, interface 204 between the processor and the cache incorporates the claimed extractor and direct memory access engine.

Regarding Claim 21, Piazza is expressly described as a system "for motion compensation of digital video data". Piazza, abstract.

Regarding Claim 23, in Piazza, fig. 2 illustrates a block diagram of the decoder. Variable length decoding module 210 is the claimed variable length decoder. Slice buffer 420 of Lee is the claimed "compressed data buffer". Inverse quantization unit 230, inverse DCT unit 240, and motion compensation unit 200 form the claimed decompression engine. In Lee, variable length decoding is described as performed per slice, or macroblock row, to use the claim language. Lee, col. 4: lines 37–43.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID N. WERNER whose telephone number is

(571)272-9662. The examiner can normally be reached on Monday-Saturday from 10:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph G. Ustaris can be reached on (571) 272-7383. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. N. W./
Examiner, Art Unit 2483

/Joseph G Ustaris/
Supervisory Patent Examiner, Art Unit 2483